IN THE CLAIMS:

1. (Amended) A built-in self-test controller, comprising a logic built-in self-test domain ~~capable of performing~~ configured to perform a logic built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test.

2. (Amended) The built-in self-test controller of claim 1, wherein the logic built-in self-test domain comprises:
   a logic built-in self-test state machine; and
   a pattern generator ~~capable of~~ configured to generating a scan pattern for use in a state of the logic built-in self-test state machine.

3. (Amended) The built-in self-test controller of claim 2, wherein the logic built-in self-test state machine ~~further comprises~~ is configured to:
   enter a reset state entered upon receipt of an external reset signal;
   enter an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;
   enter a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;
   enter a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and
   enter a done state entered into from the step state when the content of the pattern generator equals the predetermined vector count.

4. (Original) The built-in self-test controller of claim 2, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

5. (Amended) The built-in self-test controller of claim 2, wherein the logic built-in self-test controller includes a register configured to store a logic built-in self-test signature, wherein the logic built-in self-test signature includes at least one of:
a bit indicating an error condition arose; and
a bit indicating whether the stored results are from a previous logic built-in self-test run.

6. (Amended) The built-in self-test controller of claim 1, further comprising a memory ~~builtin~~ built-in self-test domain.

7. (Original) A built-in self-test controller, comprising a logic built-in self-test domain including means for performing a logic built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test.

8. (Amended) The built-in self-test controller of claim 7, wherein the means for performing the logic built-in self-test comprises:
a logic built-in self-test state machine; and
a pattern generator ~~capable of generating~~ configured to generate a scan pattern for use in a state of the logic built-in self-test state machine.

9. (Amended) The built-in self-test controller of claim 7, further comprising a memory ~~builtin~~ built-in self-test domain.

10. (Amended) An integrated circuit device, comprising:
a plurality of memory components;
a logic core;
a testing interface; and
a built-in self-test controller controlled through the testing interface, comprising a logic built-in self-test domain ~~capable of performing~~ configured to perform a logic built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test.

11. (Amended) The integrated circuit device of claim 10, wherein the logic built-in self-test domain comprises:

a logic built-in self-test state machine; and

a pattern generator ~~capable of generating~~ configured to generate a scan pattern for use in a state of the logic built-in self-test state machine.

12. (Amended)The integrated circuit device of claim 11, wherein the logic built-in self-test state machine ~~further comprises~~ is configured to:

enter a reset state entered upon receipt of an external reset signal;

enter an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;

enter a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;

enter a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and

enter a done state entered into from the step state when the content of the pattern generator equals the predetermined vector count.

13. (Original) The integrated circuit device of claim 11, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

14. (Amended) The integrated circuit device of claim 11, wherein the logic built-in self-test controller includes a register configured to store a logic built-in self-test signature, wherein the logic built-in self-test signature includes at least one of:

a bit indicating an error condition arose; and

a bit indicating whether the stored results are from a previous logic built-in self-test run.

15. (Original) The integrated circuit device of claim 10, wherein the built-in self-test controller further comprises a memory built-in self-test domain.

16. (Original) The integrated circuit device of claim 10, wherein testing interface comprises a Joint Test Action Group tap controller.

17. (Amended) An integrated circuit device, comprising:
a plurality of memory components;
a logic core;
a testing interface; and
means for performing a logic built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic ~~builtin~~ built-in self-test.

18. (Amended) The integrated circuit device of claim 17, wherein the performing means comprises:

a logic built-in self-test state machine; and
a pattern generator ~~capable of generating~~ configured to generate a scan pattern for use in a state of the logic built-in self-test state machine.

19. (Amended) The integrated circuit device of claim 17, wherein the ~~built-in self-test controller~~ means for performing the logic built-in self test further comprises a memory built-in self-test domain.

20. (Original) The integrated circuit device of claim 17, wherein testing interface comprises a Joint Test Action Group tap controller.

21. (Amended) A method for performing a built-in self-test on an integrated circuit device, comprising:
externally resetting a built-in self-test controller including a logic built-in self-test engine;
performing a logic built-in self-test from the built-in self-test controller at a test frequency at least as slow as a slowest frequency of a plurality of timing

domains to undergo the logic built-in self-test; and

obtaining the results of the ~~performed~~ logic built-in self-test.

22. (Original) The method of claim 21, wherein resetting the built-in self-test controller includes initializing a multiple input signature register and a pattern generator.

23. (Amended) The method of claim 21, wherein performing the logic built-in self-test includes:

initiating a plurality of components and signals in a logic built-in self-test domain of the ~~dual mode~~ built-in self-test controller upon receipt of a logic built-in ~~selftest~~ self-test run signal;

scanning a scan chain upon the initialization of the components and the signals; stepping to a new scan chain; and

repeating the previous scanning and stepping until the content of a pattern generator equals a predetermined vector count.

24. (Amended) The method of claim 23, further comprising at least one of:

setting a bit in ~~the~~ a multiple input signature register in the built-in self-test controller indicating an error condition arose; and

setting a bit in the multiple input signature register indicating whether the stored results are from a previous logic built-in self-test run.

25. (Amended) The method of claim 21, wherein externally resetting a built-in self-test controller includes resetting a built-in self-test controller including a memory built-in self-test engine and the method further comprises:

performing a memory built-in self-test from the built-in self-test controller; and obtaining the results of the ~~performed~~ memory built-in self-test.

26. (Amended) A method for testing an integrated circuit device, comprising: interfacing the integrated circuit device with a tester;

externally resetting a built-in self-test controller including a logic built-in self-test engine;

performing a logic built-in self-test from the built-in self-test controller at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test; and

obtaining the results of the ~~performed~~ logic built-in self-test.

27. (Original) The method of claim 26, wherein resetting the built-in self-test controller includes initializing a multiple input signature register and a pattern generator.

28. (Amended) The method of claim 26, wherein performing the logic built-in self-test includes:

initiating a plurality of components and signals in a logic built-in self-test domain of the ~~dual mode~~ built-in self-test controller upon receipt of a logic built-in ~~selftest~~ self-test run signal;

scanning a scan chain upon the initialization of the components and the signals; stepping to a new scan chain; and

repeating the previous scanning and stepping until the content of a pattern generator equals a predetermined vector count.

29. (Amended) The method of claim 28, further comprising at least one of:

setting a bit in ~~the~~ a multiple input signature register in the built-in self-test controller indicating an error condition arose; and

setting a bit in the multiple input signature register indicating whether ~~the stored~~ results stored thererin are from a previous logic built-in self-test run.

30. (Amended) The method of claim 26, wherein externally resetting a built-in self-test controller includes resetting a built-in self-test controller including a memory built-in self-test engine and the method further comprises:

performing a memory built-in self-test from the built-in self-test controller; and

obtaining the results of the ~~performed~~ memory built-in self-test.

31. (Original) The method of claim 26, wherein obtaining the results includes reading at least one of a logic built-in self-test signature and a memory built-in self-test signature.

32. (Original) The method of claim 26, wherein interfacing the integrated circuit device with the tester includes employing Joint Test Action Group protocols.